Notice of Allowability	Application No.	Applicant(s)	
	10/606,419	SINGHAL ET AL.	
	Examiner	Art Unit	
	Tuyen To	2825	TT

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☒ This communication is responsive to *01/09/2006*.

2. ☒ The allowed claim(s) is/are *6,8,9,11,13,14,16-20, 22-29, and 31-37; renumbered (37 CFR 1.126)*.

3. ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
   a) ☐ All b) ☐ Some* c) ☐ None of the:
      1. ☐ Certified copies of the priority documents have been received.
      2. ☐ Certified copies of the priority documents have been received in Application No. _____ .
      3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

   * Certified copies not received: _____.

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.
THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.

4. ☐ A SUBSTITUTE OATH OR DECLARATION must be submitted. Note the attached EXAMINER'S AMENDMENT or NOTICE OF INFORMAL PATENT APPLICATION (PTO-152) which gives reason(s) why the oath or declaration is deficient.

5. ☒ CORRECTED DRAWINGS (as "replacement sheets") must be submitted.
   (a) ☒ including changes required by the Notice of Draftsperson's Patent Drawing Review (PTO-948) attached
      1) ☒ hereto or 2) ☒ to Paper No./Mail Date *07/12/2005*. (For Figures 1-5)
   (b) ☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date _____.

Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).

6. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)

1. ☐ Notice of References Cited (PTO-892)
2. ☒ Notice of Draftperson's Patent Drawing Review (PTO-948)
3. ☐ Information Disclosure Statements (PTO-1449 or PTO/SB/08), Paper No./Mail Date _____
4. ☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material
5. ☐ Notice of Informal Patent Application (PTO-152)
6. ☐ Interview Summary (PTO-413), Paper No./Mail Date _____ .
7. ☒ Examiner's Amendment/Comment
8. ☒ Examiner's Statement of Reasons for Allowance
9. ☐ Other _____.

A. M. Thompson
Primary Examiner
Technology Center 2800

DETAILED ACTION

1. This is a response to the amendment and remarks/arguments filed on 01/09/2006.

2. Claims 1-5, 7,10,12,15,21,30, and 38-40 are cancelled.

3. Claims 6, 8, 9, 11, 13, 16, 18, 20, 23, 25-29, and 31- 37 are amended.

4. Claims 6, 8, 9, 11, 13,14, 16-20, 22-29, and 31-37 are pending.

5. The amended drawings for Figs. 6-16 have been approved.

6. The amended title has been approved.

7. The amended specification has been approved

8. Applicant's remarks/arguments filed 01/09/2006 are considered persuasive and obviates all outstanding claim rejections. Accordingly, claims 6, 8,9, 11, 13,14, 16-20, 22-29, and 31-37 are allowed.

EXAMINER'S AMENDMENT

9. An examiner's amendment to the record appears below. Should the changes and/or additions be unacceptable to applicant, an amendment may be filed as provided by 37 CFR 1.312. To ensure consideration of such an amendment, it MUST be submitted no later than the payment of the issue fee.

10. Authorization for this examiner's amendment was given in a telephone interview with John McNelis (Reg. No. 37186) on 01/31/2006.

11. The application has been amended as follows:

In the claims

Claim 6, line 9, replace "in false" with --in a determination that the analysis region is not verified--

Claim 6, line 12, replace " the articulated fan-in" with -- an articulated fan-in--.

Claim 8, line 9, replace "in false" with --in a determination that the analysis region is not verified--

Claim 8, line 15-16, replace "the plot window" with --a plot window--

Claim 9, line 9, replace "in false" with --in a determination that the analysis region is not verified--

Claim 9, line 10, replace "the plot window" with --a plot window-- .

Claim 9, line 12, replace "the reset portion" with --a reset portion-- .

Claim 11, line 9, replace "in false" with --in a determination that the analysis region is not verified--

Claim 11, line 12, replace "and/or adding the articulated fan-in " with --or adding an articulated fan-in --

Claim 13, line 8, replace "in false" with --in a determination that the analysis region is not verified--

Claim 13, line 9, replace "the plot window" with --a plot window--

Claim 16, line 9, replace "is false" with --results in a determination that the circuit design is not verified--

Claim 17, line 1, delete "automatically"

Claim 18, line 9, replace "is false" with --results in a determination that the circuit design is not verified--

Claim 19, line 4, replace "the productivity weights" with --productivity weights-- .

Claim 20, line 8, replace "is false" with -- results in a determination that the circuit design is not verified--

Claim 23, line 9, replace "is false" with -- results in a determination that the circuit design is not verified--

Claim 25, line 9, replaced "is false" with --results in a determination that the circuit design is not verified--

Claim 26, line 8, replace "is false" with --results in a determination that the circuit design is not verified--

Claim 28, line 11, replace "is false" with --results in a determination that the circuit design is not verified--

Claim 29, line 9, replace "the digital design" with --the circuit design--

Claim 31, line 10, replace "the verified user defined rules" with --verified user defined rules--

Claim 32, line 10, replace "the verified user defined rules" with --verified user defined rules--

Claim 33, line 10, replace "the verified user defined rules" with --verified user defined rules--

Claim 34, line 10, replace "the verified user defined rules" with --verified user defined rules--

Allowable Subject Matter

12. **Claims 6, 8, 9, 11, 13,14, 16-20, 22-29, and 31-37** are allowed.

13. The following is an examiner's statement of reasons for allowance:

14. **Claims 6, 8, 9, 11, 13, and 14** are allowable because the prior art of record does not teach or fairly suggest a method for guiding formal verification for a circuit design in circuit simulation software to optimize the time required for verification of the circuit design, comprising: manually modifying the analysis region if verification of the circuit design over the analysis region results in a determination that the analysis region is not verified; relating to the signal in the analysis region including adding an articulated fan-in driving the signal to the analysis region by identifying the articulated fan-in of the signal by traversing the circuit design backwards from the signal until a signal from the group consisting of primary inputs, storage elements, and articulation points is encountered; selecting a signal in a Plot window; adding a reset portion of an articulated fan-in of the selected signal in the analysis region; the user selecting an articulation point inside the analysis region; removing an articulated fan-in of the articulation point from the analysis region or adding an articulated fan-in driving the selected articulation point to the analysis region; the user selecting at least one signal in the analysis region from a Plot window, wherein each signal is selected at a specific time cycle; generating a triple based on each selected signal, wherein a triple comprises the name of the selected signal, the specific time cycle of selection and the value of the selected signal at the specific time cycle; generating a rule based on the triples; verifying the rule separately; and verifying the circuit design using the rule as an assumption for the analysis region.

15. **Claims 16-20, 22-29, and 31-37** are allowable because the prior art of record does not teach or fairly suggest a method and a system for guiding formal verification for a circuit design in circuit simulation software to optimize the time required for verification process, comprising: identifying candidate signals for modification of the analysis region if verification of the circuit design results in a determination that the circuit design is not verified; identifying articulation points corresponding to the analysis region as the candidate signals; automatically modifying the analysis region using the candidate signals ; prioritizing the candidate signals on the basis of productivity choices; expanding the analysis region by including the an articulated fan-in corresponding to the highest-productivity choices that are located at the boundary of the analysis regions; removing the articulated fan-in corresponding to the highest-productivity choices that are located inside the analysis region from the analysis region; manually modifying the analysis region if there are no appropriate candidate signals; defining an abstraction created in response to the low productivity choices in the analysis region; proving the abstraction in the circuit design separately; verifying the circuit design using the abstraction in the analysis region; defining an assumption created in response to low productivity choices in the analysis region; by proving the assumption in the circuit design separately; verifying the circuit design using the assumption in the analysis region; the user selecting at least one signal in the analysis region from a Plot window, wherein each signal is selected at a specific time cycle; generating a triple based on each selected signals, wherein a triple comprises the name of the selected signal, specific time cycle of selection and the value of the selected signal at the specific time

cycle; generating a rule based on the triples; verifying the rule separately; verifying the circuit design using the rule as an assumption for the analysis regions; verifying the circuit design by applying formal verification over the analysis region including having a user deciding that there is an error in the circuit design in case there are no high-productivity choices; identifying an analysis region for verifying the circuit design; verifying the circuit design by applying formal verification over the analysis region; identifying articulation points corresponding to the analysis region as analysis region modification choices; and automatically modifying the analysis region using an articulated fan-in of the analysis region modification choices if verification of the circuit design over the analysis region results in a determination that the analysis region is not verified.

16. Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

Conclusion

17. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Tuyen To whose telephone number is (571) 272-8319. The examiner can normally be reached on 9:00am-5:00pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Jack Chiang can be reached on (571) 272-7483. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Tuyen To

Patent examiner

AU 2825

A. M. Thompson
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